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NASA CONTRACTOR
REPORT

NASA CR-150069

IMPLEMENTATION OF LARGE SCALE INTEGRATED (LSI) CIRCUIT
DESIGN SOFTWARE

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September 16, 1976

Final Report



Prepared for

NASA - GEORGE C. MARSHALL SPACE FLIGHT CENTER
Marshall Space Flight Center, Alabama 35812

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16. ABSTRACT This document describes the work performed to modify and update portions of the Computer Aided Design and Test system, a collection of Large Scale Integrated (LSI) circuit design programs. Major modifications were made to the Mask Analysis Program (MAP) in the form of additional operating commands and file processing options. Modifications were also made to the Artwork Interactive Design System (AIDS) to correct some deficiencies in the original program as well as to add several new command features related to improving the response of AIDS when dealing with large files. The remaining work was concerned with updating various programs within CADAT to incorporate the Silicon on Sapphire (SOS) Silicon Gate Technology.			
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PREFACE

This report formally documents the work performed by M&S Computing, Inc., under Contract No. NAS8-31358, "Implementation of Large Scale Integrated (LSI) Circuit Design Software," for the George C. Marshall Space Flight Center of the National Aeronautics and Space Administration.

Included is a discussion of the work performed and recommendations for further development of the Design Automation System.

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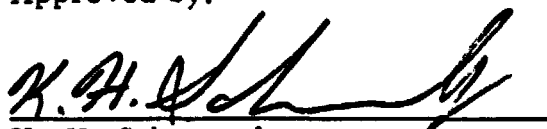

K. H. Schonrock

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LIST OF ACRONYMS

AIDS	Artwork Interactive Design System
CADAT	Computer Aided Design and Test
CMOS	Complementary Metal Oxide Semiconductor
DBMS	Data Base Management System
DJANAL	Disjunct Analyzer
FETLOG	Combined FETSIM and LOGSIM Processor
FETSIM	FET Circuit Simulation Program
LOGSIM	Logic Simulation Program
LSI	Large Scale Integrated
MAP	Mask Analysis Program
MOS	Metal Oxide Semiconductor
MOSFET	MOS Field Effect Transistor
MP2D	Multiple Port 2-Dimensional
PCB	Printed Circuit Board
PMOS	P-Channel MOS
PRF	Place, Route, and Fold
PR2D	Place and Route 2-Dimensional
SOS	Silicone on Sapphire
TPG (LASAR)	Test Pattern Generation Program

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1. INTRODUCTION

This final report summarizes the work done by M&S Computing under Contract No. NAS8-31358, which consisted of developing additions and modifications for the Computer Aided Design and Test (CADAT) system, a collection of Large Scale Integrated (LSI) circuit design programs. The CADAT system was designed and implemented by the Technology Division to provide a man-in-the-loop hardware/software computer facility capable of designing and testing Metal Oxide Semiconductor (MOS)/LSI arrays in the shortest possible time. CADAT offers data, counsel, and guidance to the user, who, in return, supplies the intuitive knowledge and skill required to take advantage of the capabilities of the system. CADAT contains the software required to enable an engineer to develop MOS/LSI arrays that are relatively inexpensive, precise, reliable, ready within a practical turnaround time, evaluated before the expense of actual fabrication, and that have test sequences prepared for automatic testers.

The work performed under this contract was prompted by the experience gained in implementing and using the initial version of the CADAT system and by the constantly emerging new MOS/LSI technologies. Major modifications were made to the Artwork Interactive Design System (AIDS) and the Mask Analysis Program (MAP) software. All components of the system currently support the Silicone On Sapphire (SOS) Silicon Gate Technology in addition to previously support technologies.

Most major programs are documented by formal reports which are explicitly identified by the reference list attached to this report. All modifications and additions to the CADAT software are reflected by revisions to published documents and by new documents produced in conjunction with the execution of this contract.

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2. DESCRIPTION OF WORK PERFORMED

Several software development tasks were addressed in the execution of NASA Contract NAS8-31358. They necessitated significant improvements in the AIDS and MAP software and a general upgrade of all components of the CADAT system in order to adequately support the Complementary MOS (CMOS), SOS, Silicon Gate Technology. A new program was also written to provide an interface between the MAP processor and the combined FETSIM and LOGSIM (FETLOG) processor. The major function of this program, which is referred to as the Disjunct Analyzer (DJANAL), is to isolate and analyze disjunct circuits so they may be simulated by the FETLOG processor. A complete description of specific modifications, development, and implementation of software in each of these areas is presented below.

2.1 MAP Modifications

In order to support the standard cell philosophy of LSI design more adequately, several new features were added to the MAP processor as outlined below:

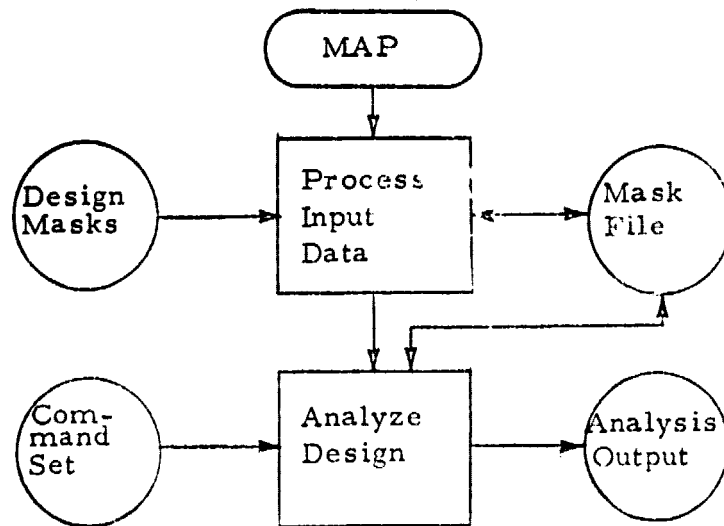
- o Addition of OPER PLAC command to provide for placing predefined cell masks in a mask analysis file.
- o Addition of a file processing option to accept mask data in MAP list format for input.
- o Addition of a file processing option to accept Banning cell library source format for input.
- o Addition of a file processing option to accept component placement data in Place, Route, and Fold (PRF) format as input.

This combination of new features provided a variety of methods for dealing with standard cell data in the MAP program. Several methods of processing mask data with and without cells are described below to illustrate the versatility of the added MAP capabilities.

2.1.1 MAP Design Analysis Without Cells

This is the most straightforward method of analysis using MAP. Figure 2-1 illustrates this flow of processing in which the input design masks represent the complete design without references to cells. The command set is formulated to test for all artwork errors and to identify nodes and devices

MAP DESIGN ANALYSIS WITHOUT CELLS



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Figure 2-1

on the complete design. A command set of this form has been created and is available for use.

2.1.2 MAP Cell Library Analysis

Although masks are normally designed using libraries of predefined artwork cells, it is advantageous to use MAP to verify the artwork of the cells whenever a new library is created or modified. The flow of such a MAP execution is illustrated in Figure 2-2. The input data consists of the cell library and a placement mask. The purpose of the placement mask is to position the cells over a design area so that they are isolated from one another. This is the same as creating a design using every cell, none of which are connected.

The command set is formulated so that the first process performed is that of placing cells according to the placement mask arrangement. The remainder of the command set performs the various artwork tests on the cells. Note that the cell library may be stored in MAP format. This will save input processing time when the cell library is required for further MAP runs.

2.1.3 MAP Design Analysis with Cells - Method 1

When masks are designed using cells, several methods of using MAP are possible. The flow of execution of one method is illustrated in Figure 2-3.

The input masks include the cell library masks and design masks which reference the cells. The command set first performs the process of placing the cells according to the design references and combining all cell placement masks with the non-cell design masks to form final composite design masks. The remainder of the command set performs analysis and identification tasks. This portion of the command set may be identical to the command set used for designs where no cells are used, since it is operating on the entire design.

2.1.4 MAP Design Analysis with Cells - Method 2

Another method of using MAP on designs with cells is illustrated in Figure 2-4. This method is somewhat more efficient than the other in that it avoids redundant testing of cells.

The input masks are the same as are the cell library masks and design masks utilized in Method 1. The command set first performs the placement of the cells and the combining of cell and non-cell masks into final composite masks. The remainder of the command set is divided into three sections. One section performs artwork analysis tasks on the non-cell portions of the

MAP CELL LIBRARY ANALYSIS

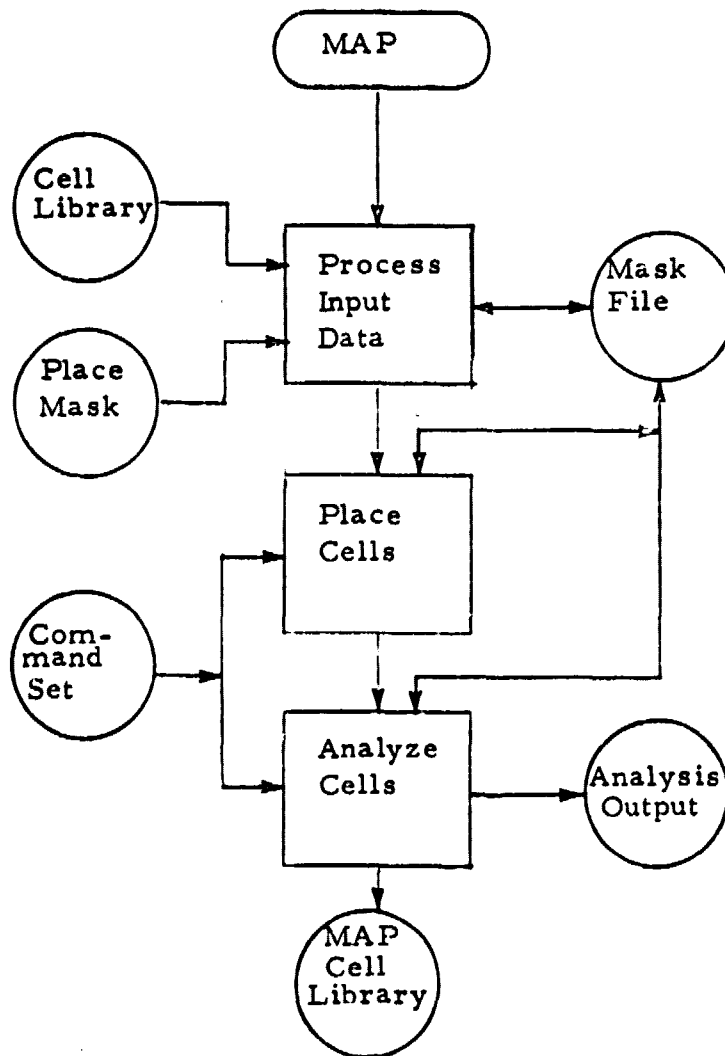


Figure 2-2

MAP DESIGN ANALYSIS WITH CELLS - METHOD 1

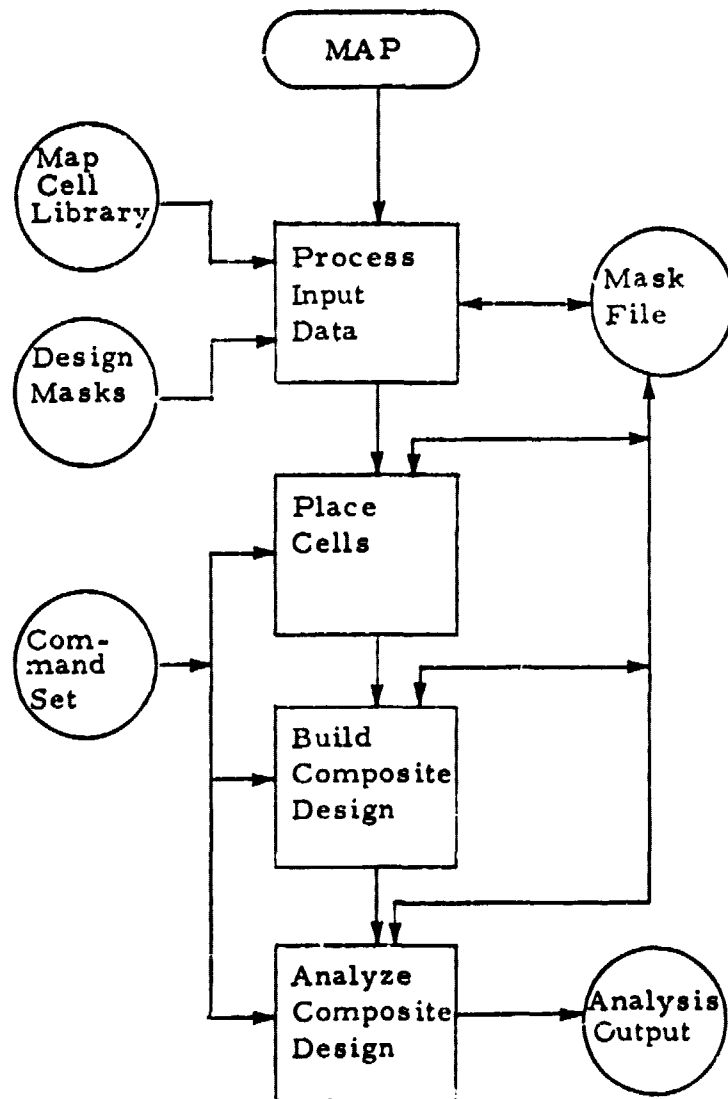


Figure 2-3

MAP DESIGN ANALYSIS WITH CELLS - METHOD 2

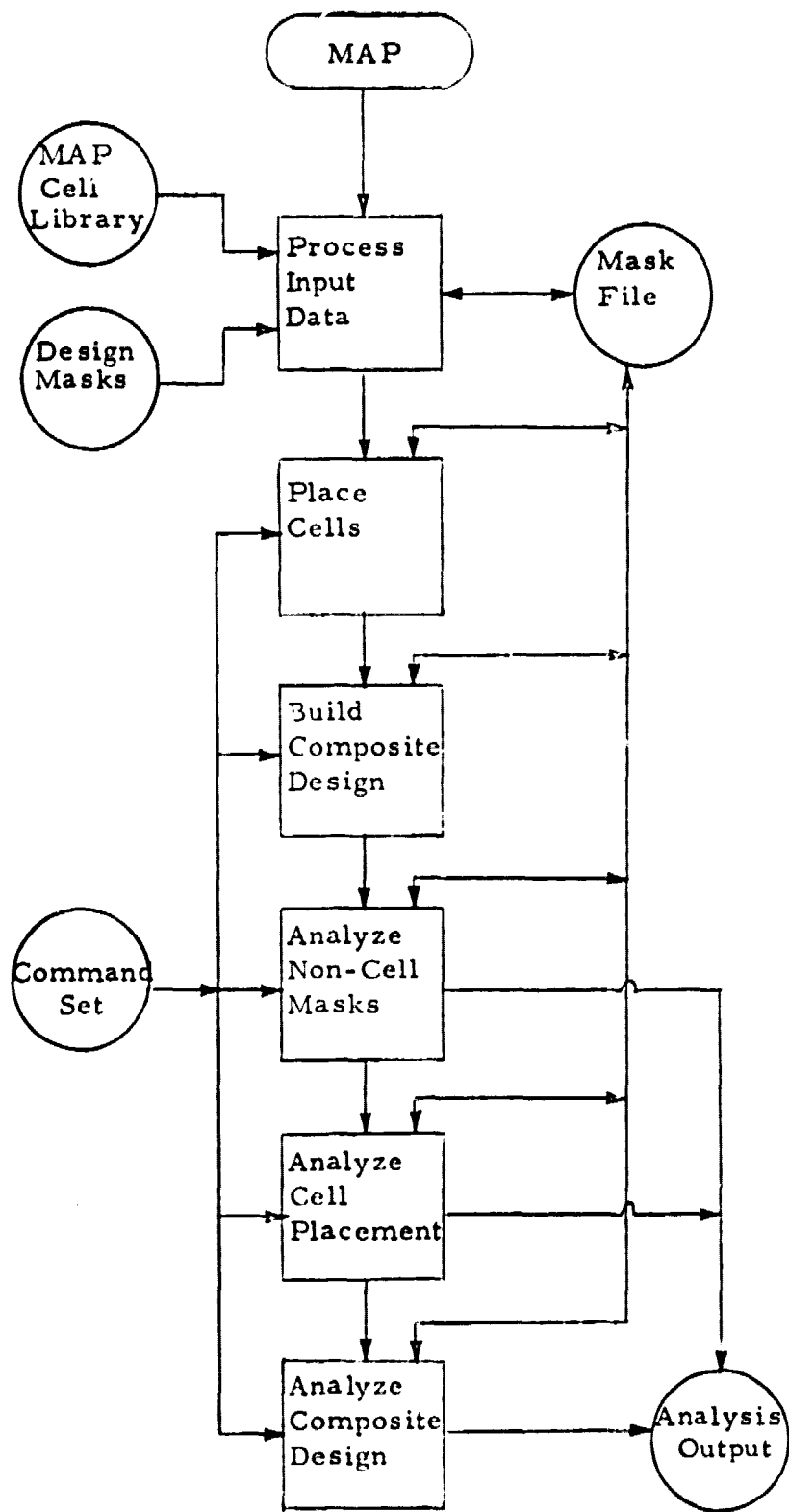


Figure 2-4

design. Another section performs analysis of the placement of the cells. The individual cell artwork need not be tested. Another section performs analysis tasks on the composite design. These tasks would be primarily node and device identification tasks and would include only those artwork tests which required a complete design. This method is the most efficient method for the analysis of designs with cells.

2.2 MAP Sigma-2 Implementation

The MAP processor has also been installed on the Sigma-2 computer with file processing options to provide an interface with the AIDS graphic system. The combination of AIDS and MAP provides the designer with a convenient means for analyzing the artwork of a LSI design in a graphic and interactive mode. It is possible to move design data freely between the two processors allowing graphic data in AIDS to be readily analyzed by MAP and allowing error masks produced by MAP to be readily observed with the AIDS display. It is expected that the MAP/AIDS software combination will prove to be an extremely effective tool for the design of LSI devices.

2.3 AIDS Modifications

The first activity in this area involved modifying AIDS to correct the following deficiencies:

- o There were problems on lines when zoomed in at a very detailed drawing scale.
- o Modification of a line node caused the other end of line node to be disturbed in some instances.
- o When performing a COPY UNIT AREA command, the placement of some cells within the unit area was being omitted.
- o Lines placed at angles other than horizontal, vertical, or forty-five degrees were being displayed in a distorted manner. (This problem was related to a system tangent routine problem and a correction to work around the problem was inserted.)
- o There was a problem concerning leaving the drawing display in delay mode and then not being able to return without reinitiating the system.

The remainder of the work on AIDS involved adding new features to enhance the system's operational capability in manipulating large design files.

The specific features so added are described below:

- o Command Interrupt - This allows the user to interrupt Place, Move, or Modify commands for window and scaling changes.
- o Modification of Last Point - This allows the user who has just placed a line, block, or shape side, to issue a reset point command. He may then reissue the point, whereupon the figure will be drawn from the previous point to this new point. The point immediately preceding this new point will then be nullified.
- o Fence File Construction - This allows the user to separate a design file into two distinct files using a fence as the dividing mechanism.
- o File Activation - This allows the user to select either the file within the fence or the file outside the fence to be active for editing. In addition, he may switch at any time to make the other file the active file.
- o Display of Files - This allows the user to call for a composite picture of both the active and inactive files at the current scale and window gain. Either the fenced or the non-fenced file may be active at the time this is done.
- o File Merging - This allows the user, when satisfied with the editing, to issue a command which will cause the two files which have been separated to merge back together.
- o Tagging of Points - This allows the user, when he creates a fenced file, to include elements lying partially within the fence. Those vertices which lie outside the fence, however, will be tagged and treated uniquely.
- o Tagged Points - Those points described above are fixed within the design file and are not movable or removable except through the use of the swap command described below.
- o Swap Command - This allows the user to replace a line containing a tagged point with another line, provided the lines have a common endpoint which has been tagged in the line to be removed. This point in the replacing line is tagged and the swapped line is removed from the design file.

- o File Biasing - This allows the user to bias all untagged points within the design file by a delta X and Y.
- o Drawing Display Compose Field Updates - This is a new feature of Sigma-2 AIDS which allows the user to update header and other information without leaving the drawing display.

The first two items above allow the designer to inject design elements with a higher degree of accuracy than was previously possible. This capability is especially useful when placing an element that covers a wide expanse yet needs to be placed very accurately. An example of such an operation is placing a metalization run to interconnect two widely spaced cells. If the viewing area is scaled to provide a display of both cells simultaneously, it is very difficult to position the interconnect with sufficient accuracy to realize a good connection. The new features alleviate this problem by allowing view window changes while the designer is in the process of placing the line that represents the connector. He can zoom in on the first cell and establish the begin point of the line, zoom in on the second cell, issue a command reset, and then establish the end point of the line. The command interrupt feature is also useful for accurate placement in a similar manner of wide ranging blocks and shapes.

The remaining items are related to improving the response of AIDS when dealing with a large design file. By separating a portion of the design into another file, the AIDS software can locate display, modify, delete, or otherwise manipulate elements at a faster rate than is possible for the entire file. The improvement in response, as would be expected, is approximately proportional to the reduction in file size. The advantage of this feature is obvious if one considers a situation in which an isolated portion of a design requires extensive modification while the remainder is essentially correct. The LSI designer is able to extract the portion of the design requiring extensive modifications, operate on it at a rapid rate, and then recombine it with the remainder of the design, thereby greatly enhancing the effectiveness of interactive operations.

The tagged point feature is provided in conjunction with the file splitting operation to assure that the relationship between the two files remains intact while they are separated. An example of the utility of tagged points is a situation in which a wiring channel must be opened up to permit additional interconnects to be made. The designer would fence the area to be moved, activate the fenced file, and bias the file by the amount required to enlarge the channel. If the move is unilateral (I. e., in the X-direction only or the Y-direction only) it is unlikely that manipulation of tagged point elements will be required. The elements that bridge the fenced area will effectively

be stretched and maintain the topological integrity of the design. If, however, a bilateral bias is applied, the bridging elements will become distorted and will very likely require modification. The swap command is employed to accomplish the modifications in such a manner that the topological integrity in this case may be also retained.

2.4 DJANAL Development

The production of DJANAL arose out of a need for a means to transform the primitive output of the MAP processor into a form suitable for use as input to the FETLOG processor. Due to its very nature, the MAP processor generates fragmentary data for each device in a design. It is therefore required that the pieces be put together to form the more commonplace lumped devices traditionally used in network simulation programs. Also, more importantly, the transistor equations generated by the MAP "BOOL" command must be analyzed to isolate and characterize disjunct circuits so that the logical function of the design may ultimately be determined.

DJANAL has been designed to allow the user to inject additional devices into the network via card input so that he may include off-chip loading or may modify the MAP generated data. A natural extension of this capability provides the facility for analyzing a network that is input manually in its entirety.

Two output files are produced by the program with an attendant listing on the printer. The first output file consists of an input file for the Logic Simulator Program (LOGSIM) portion of the FETLOG processor. This file will consist of at least one ROM card and an accompanying NET card for each disjunct circuit in the design. The disjuncts that have more than one output will have a ROM and a NET card for each such output. The second output file consists of a collection of input decks to the FET Circuit Simulation Program (FETSIM) portion of the FETLOG processor. There will be one FETSIM deck for each disjunct circuit in the design.

DJANAL has been designed to accept parametric and excitation data in an attempt to relieve the user of the burden of injecting this data at FETLOG run time. It is anticipated that editing of DJANAL output prior to running FETLOG will be unnecessary.

2.5 System Support

Several minor tasks related to improving the performance of existing software and upgrading existing software to support new design technologies were performed as delineated below:

- o Several hitherto unknown bugs in the LOGSIM software have been identified and corrected.
- o An error in the Place and Route 2-Dimensional (PR2D) I/O routine caused erroneous mapping of global design data into the final PR2D output. The error has been corrected, and a significant improvement on the final output of PR2D has been obtained.
- o The first release of the Multiple Port 2-Dimensional (MP2D) Layout has been installed on the Sigma-5 computer. Test case results indicate that it is approximately 90% operational. Further work is awaiting delivery of a MP2D cell library and a copy of the test case results obtained by RCA.
- o The SOS version of PR2D has been installed on the Sigma-5 and appears to run satisfactorily.
- o The SOS version of FETSIM has been installed on the Sigma-5 and appears to run satisfactorily. Several modifications were required to get the printer plot feature to operate properly.

3. RECOMMENDATIONS FOR FUTURE DEVELOPMENT

In considering candidate areas for CADAT system improvement, one must first recognize the current capability of the system with respect to the tasks that can be performed and the ease by which these tasks can be brought to bear on the design problem. With respect to identifying the tasks that can be performed (i.e., the available software), a summary of the purpose and function of each individual component in the CADAT system is presented in Section 3.1. The ease of use of the CADAT system is currently relatively unknown and a plan is set forth in Section 3.2 that is designed to pinpoint possible inadequacies of the system and to identify bottlenecks in the design process. The subject of CADAT system general improvements, which should be attacked only after the proposed system testing outlined in Section 3.2 is performed, is addressed in Section 3.3. Finally, Section 3.4 outlines a variety of improvements and new features for the individual processors that should be of certain benefit to the effectiveness of the CADAT system.

3.1 CADAT System Overview

Presented in this section is an overview of the software components that comprise the CADAT system in its current state. These components are classified in four different categories - layout, analysis, graphics, and interface - to reflect the general area of applicability.

3.1.1 Automatic Layout Programs

PRF	1-dimensional P-Channel MOS (PMOS) and CMOS LSI circuit layout.
PR2D	2-dimensional CMOS and SOS LSI circuit layout.
MP2D	2-dimensional CMOS and SOS LSI circuit layout.
PCB	Hybrid and printed circuit layout.

3.1.2 Analysis Programs

LOGSIM	Logic Simulation Program (discrete time).
FETSIM	FET Circuit Simulation Program (continuous time).
FETLOG	Combined LOGSIM and FETSIM.
TPG (LASAR)	Test Pattern Generation Program.
MAP	Mask Analysis Program.

3.1.3 Graphics Programs

AIDS Interactive Graphics Display and Editing.

DSPLIB Display Librarian.

3.1.4 Interface Programs

ARTWORK Gerber Plotter Mask Generation.

MANART Mann Pattern Generator Artwork Generation.

PCBART PCB Mask Interface to Gerber Plotter.

BCCP Interface to Gerber 700 Plotter.

PRFAID Interface between PRF Formatted Data and AIDS
Graphic Display System.

CARD Interface between TPG and H316 Tester.

NTRAN Interface between PRF (or PR2D) Input Data
Format and LOGSIM and L TPG (LASAR) Input
Formats.

TPGITF Interface between TPG (LASAR) Output Format
and Macrodata-200 Tester Input Format and
LOGSIM Input Format.

EDIT Card Image Edit Utility Program.

3.2 CADAT System Testing

It is proposed that the CADAT system be methodically exercised in the near future in order to gain a better understanding of the overall effectiveness of the software.

Since CMOS and SOS are currently the favored technologies for LSI design development, it appears that the CADAT system could be best exercised by selecting designs in each of the two technologies and subjecting them to each process path (design intent and design verification) in the system. Since the CMOS MAP command set has already been developed, it is suggested that the system be tested first with CMOS; and then, with the experience gained, the system would be tested with an SOS design. The design types selected should be sufficiently diverse (sequential versus non-sequential) to gauge the

performance of the system with regard to the peculiarities of each type. As each of the above proposed tests is performed, a more substantial understanding of the ease with which a design description may be transferred from one process to another will be obtained. This knowledge will help formulate requirements for the CADAT Executive and the unified data base, which are briefly discussed in Section 3.3.

3.3 CADAT System General Improvements

This section outlines additions of a general nature to the CADAT software that are considered by the contractor to promise a general improvement in system usability. Two items are proposed: a system executive and a more unified data base. A more coherent and consistent means for utilizing the CADAT software might thus be realized.

3.3.1 CADAT Executive

A CADAT Executive system is proposed that can provide maximum use convenience and at the same time allow tight control of design information and of standard system processors. Extensive system journaling can be provided to permit an accurate history of the designs that have been processed by the CADAT Executive. Although it is possible and potentially desirable to utilize a general purpose Data Base Management System (DBMS) to implement the Executive, the contractor is not yet in a position either to recommend or condemn it for that purpose. All that is proposed is the language and file management scheme described below.

Salient features of the Executive would be:

- o A standardized and rigid file naming scheme by which the identify and purpose of a file can be readily ascertained, and which will facilitate automatic setup of job runstreams.
- o A user's language whereby the user enters a design description and commands the Executive to apply any one or more standard system processors.
- o A system manager language whereby the system manager installs standard system processors and standard system libraries.

3.3.2 Data Base Unification

The subject of data base integration for CAD has received much attention by the industry recently and is generally regarded as an essential

element for an efficient system. The use of a common mechanism for extracting information pertaining to the particular design technology applied to a particular design assures that each processor in the system is dealing with consistent design data. Korewack and Teger (pages 399-406, 14th Annual Design Automation Conference Proceedings) have published a good treatment of the manner in which the data base might be structured in order to realize a complete and flexible design system. They describe a hierarchically structured system with which the geometric, logical, and electronic attributes of a design can be consistently referenced. Figure 3-1 illustrates the essence of such a data structure. The character of each entity (chip, standard cells, gates, devices) can be determined as a function of its constituent items and the manner in which they are interconnected. These items are strung together in the data base so that an entity may be identified as a subelement of any other entity higher up in the structure. This capability provides a means for identifying an element quite specifically. For example, a particular transistor is easily identified as being a subelement of each of a specific gate and standard cell element. This concept, just as the CADAT Executive, may be materialized by utilizing a general purpose DBMS or by developing special software. The special software could be implemented with standard FORTRAN IV and would probably be more transportable and efficient than the general purpose DBMS. It is emphasized that a conclusion on this issue cannot be drawn without further study.

3.4 Application Software Improvement

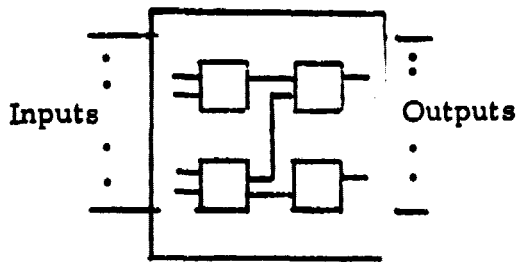
Presented below is a brief discussion of modifications or additions to specific CADAT software modules that can be made to improve individual performance and utility.

- o FETLOG - Provide capability to accept and store logic expressions as the functional definition of an ROM. This feature could eliminate the lengthy bit tables that are currently required to define ROM models having many inputs.
- o FETLOG - Provide capability to represent signals in transition as unique logic "states" (positive going, negative going). This would provide a more adequate means for simulating edge-triggered devices.
- o DJANAL - Provide capability to recognize cross-coupled disjuncts and formulate a pseudo-disjunct for use in FETLOG. This can potentially ease the processing load on FETLOG by virtue of the fact that a cross-coupled pair of disjuncts typically represent a flip-flop, a device which should obviously be simulated intact.

- o FETSIM - It is suggested that either a replacement for FETSIM be found or that an entirely new program be written to perform its function. Even though the FET model has been successively updated over the years to support emerging technologies, the numerical integration technique and the matrix inversion technique remain as they were when FETSIM was first implemented (circa 1965). Needless to say, numerical integration and matrix inversion algorithms have been significantly improved over the past ten years and could provide for a pronounced reduction in the computer time required for MOS Field Effect Transistor (MOSFET) network analysis. This improvement in performance is especially desirable in the FETLOG environment where many analog simulations may be in execution simultaneously.
- o PCB - The automated Printed Circuit Board (PCB) layout programs are considered to be the most difficult of the CADAT programs to use. The Placement, Organizer, and Router processors are inflexible and relatively inefficient in their use of computer time and memory. It is recommended that a long range program for re-writing these processors be undertaken. Design of the total system should be established, followed by incremental implementation of the Router, Organizer, and Placement processors. The PCB input processor appears inadequate in its current form.

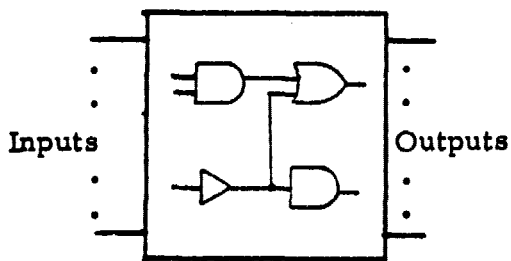
In addition to these listed specific improvements, the CADAT system software as a whole should be examined with respect to transportability to other computer systems. Although all new software has been written with transportability as a design objective, there are wide variations in the difficulty with which the programs may be implemented on other computers. Efforts expended in this area could range between that required to document problems for users to modifying programs or maintaining multiple versions of programs.

LSI FUNCTIONAL HIERARCHY



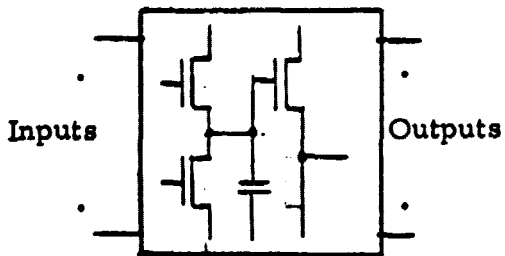
LSI CHIP

Outputs = Function of Inputs, Cells,
Nets.



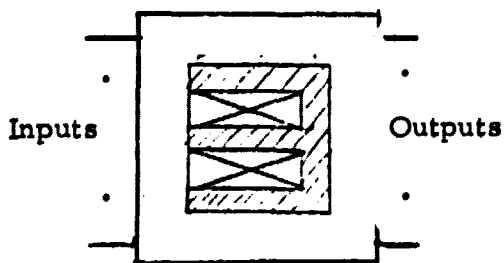
Standard Cell

Outputs = Function of Inputs, Gates,
Nets.



Gate

Outputs = Function of Inputs, Devices,
Nets.



Device

Outputs = Function of Inputs, Masks.

Figure 3-1

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